Accurate Thermal Simulation of 3DIC Package with Co-Packaged Optics

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62 THE CHIPS TO SYSTEMS CONFERENCE

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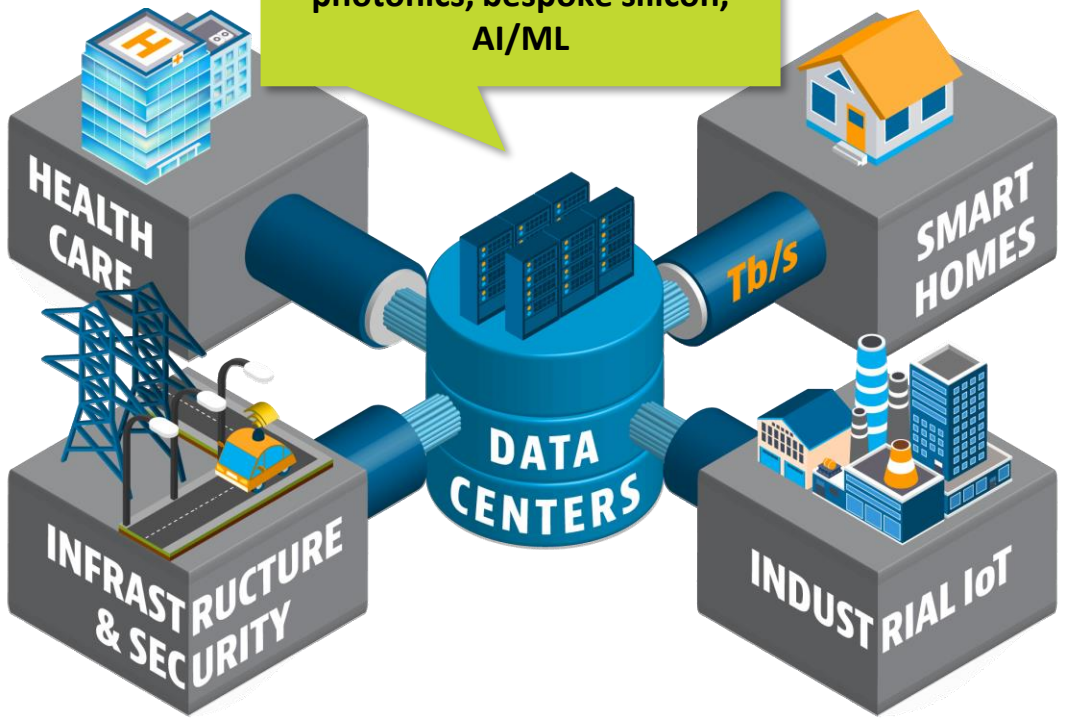
Consumer electronics, smart phone sensors, IoT home sensors, displays, …

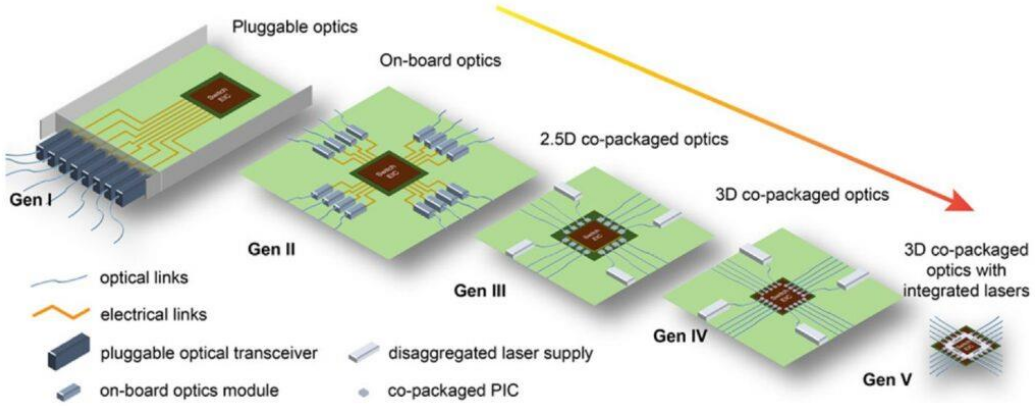


5G/6G, Optical communications, analog & RF systems, structural & environmental sensors, autonomous vehicle navigation (LIDAR), …

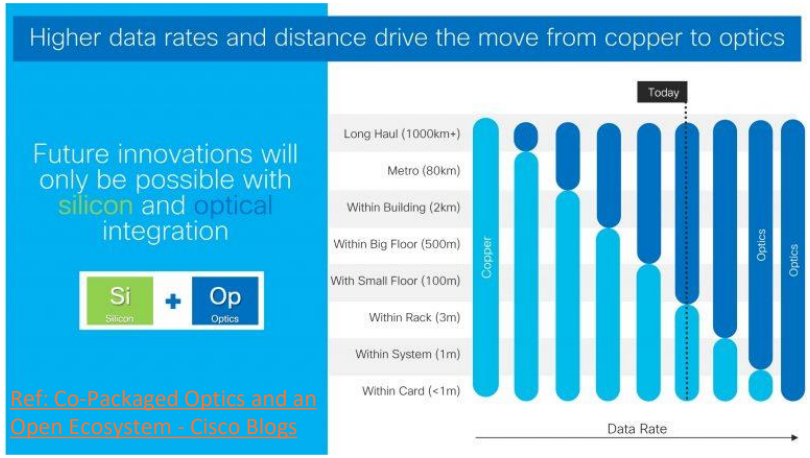
Industrial IoT, industrial chemical & environmental sensing, …

Why Co-Packaged Optics?

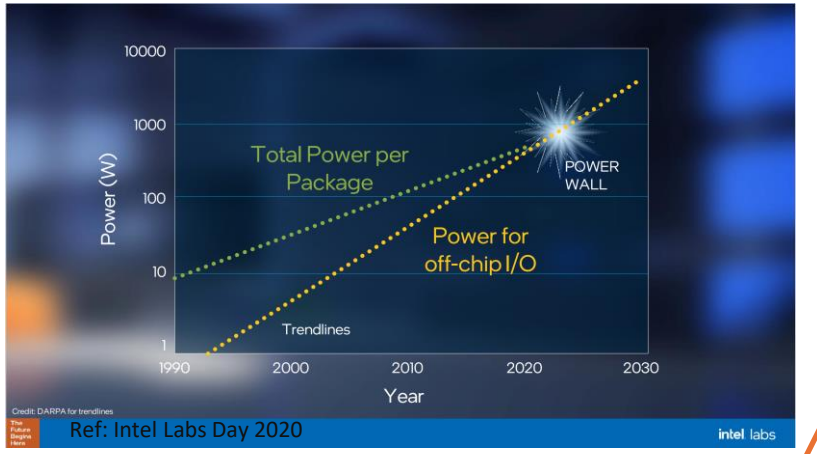
- Traditional Cu interconnects cannot scale to current requirements
- Optical interconnects will continue to replace copper
- Current optical interconnects provide increased scalability, but power/cost requirements become untenable
- Co-packaged optics brings power and cost down and allows for breaking through the “power wall”
- Challenge from tighter integration → increased thermal power density, Increased thermal crosstalk between dies.



Ref: “Perspective on the future of silicon photonics and electronics” N. Margalit, et.al., Appl. Phys. Lett. 118, 220501 (2021)



Ref: Co-Packaged Optics and an Open Ecosystem - Cisco Blogs



Ref: Intel Labs Day 2020

Motivation

- Need:
  - Thermal simulation solutions needed for 3DIC packages with co-packaged optics.
- Challenge:
  - Large HPC requirement for performing physical simulation of entire multi-die stack
  - Photonic integrated circuit (PIC) poses additional challenge that cannot be addressed with traditional semiconductor design flows
  - New workflow needed to account for thermal impact on overall performance
- Solution:
  - Use reduced order models (ROMs) of electrical IC (EIC) and PIC for efficient but accurate thermal simulation of 3DIC package.
  - ROM needs to capture the curvilinear geometry of photonic components in PICs which are unique from typical geometries found in EICs.
  - Optimize 3DIC architecture to improve cooling and reduce thermal effects.
  - Import temperature map from thermal simulation into EIC and PIC design process for thermally aware circuit design.

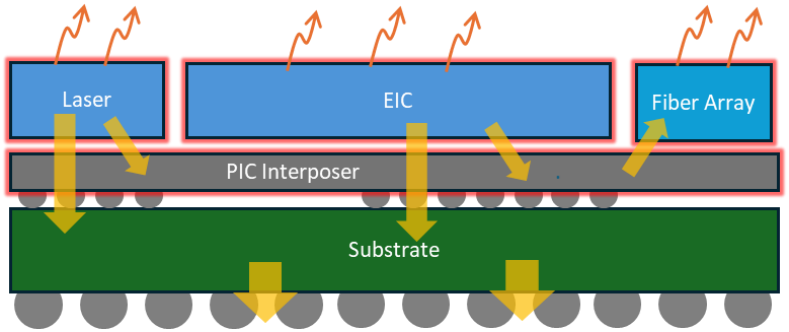


Figure: Thermal sources in a CPO package.

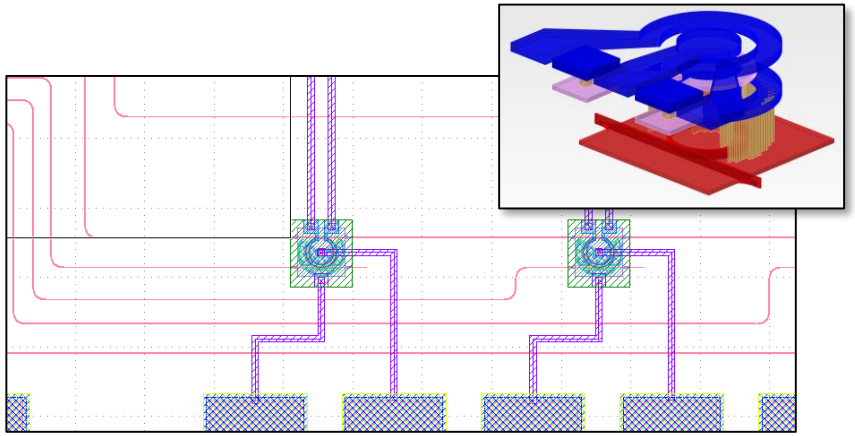
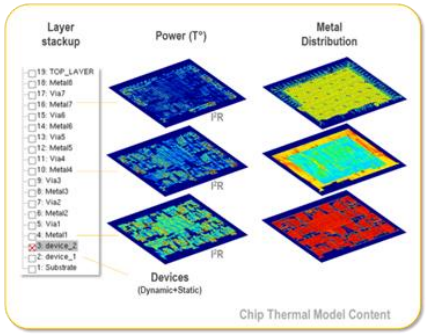


Figure: Curvilinear waveguides and heater in a photonic circuit.

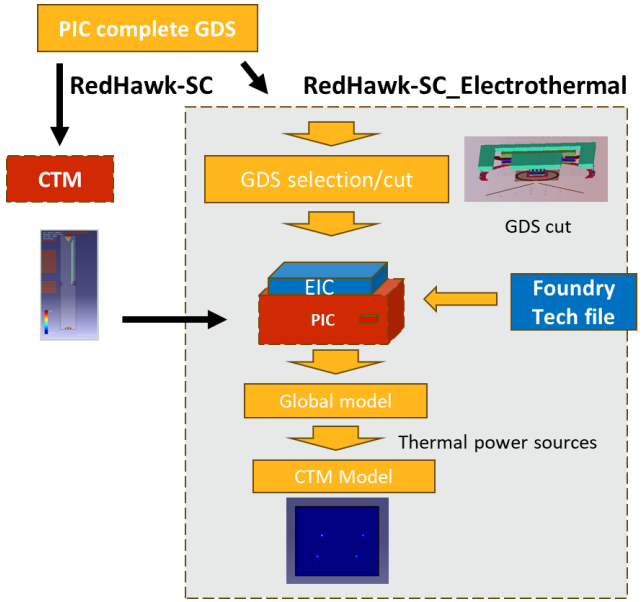
Thermal Simulation of 3DIC Package with Hybrid Chip Thermal Model

- Use ROMs for modelling EIC and PIC
  - Chip Thermal Model (CTM) is a temperature-dependent, layer-aware chip power map library [1].
- Use of CTM as a ROM of EIC and PIC enables accurate yet computationally efficient thermal simulation of multi-die package.
- Photonic layout contains curvilinear geometries, e.g., waveguides and ring heaters that needs to be modeled accurately in a traditional CTM (used in EIC design)
  - Combine CTM with curvilinear geometry patterns from important layers of the PIC GDS for thermal simulation of the PIC.
- Foundry tech file provides information for stacking EIC/PIC dies for generation of a complete CTM for thermal simulation



Chip Thermal Model

- Temperature dependent leakage power
- Per layer tile metal density
- Included power-thermal feedback



[1] Thermal Solutions for 3-D IC, Packages and System - Whitepaper

Thermal Simulation Workflow

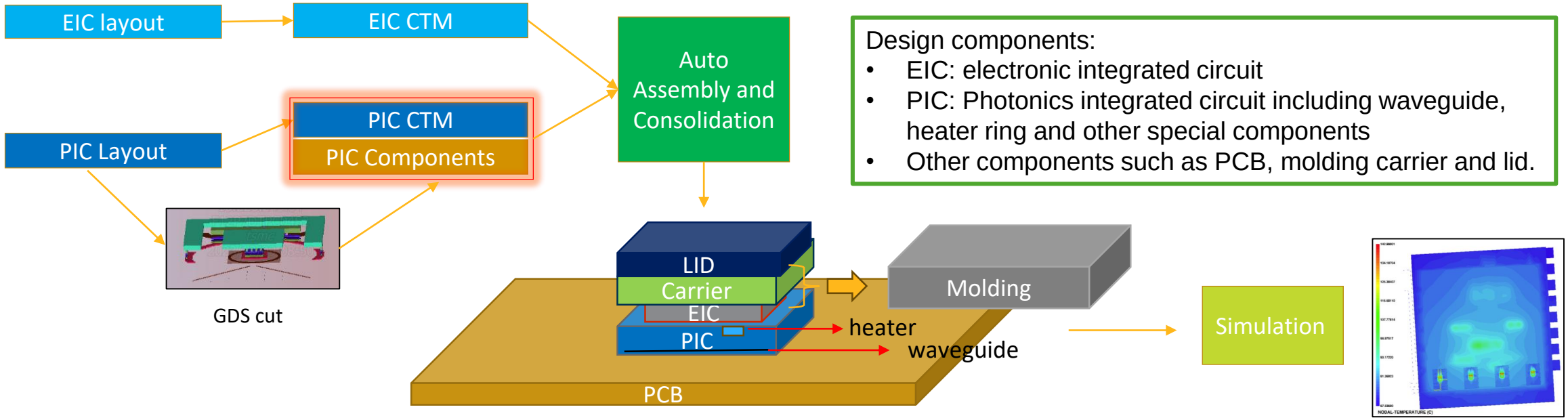


Figure: Thermal simulation workflow based on a generic 3DIC package with CPO.

- Highlights:
  - Computationally efficient due to use of CTMs
  - Accurate thermal map for PIC by preserving geometries of critical photonic components
  - Automated flow for stacking/aligning multi-die package

Application: Thermally Aware PIC Simulation

- Import temperature map from thermal simulation into photonic circuit simulator
- Use thermally aware compact models for photonic components. E.g., ring resonators in receivers (highlighted in dashed yellow box below)
- Capture shift in ring resonance due to temperature increase from thermal cross-talk
- Thermally aware component simulation provides impact of package temperature on performance (e.g., shift in grating coupler spectrum)

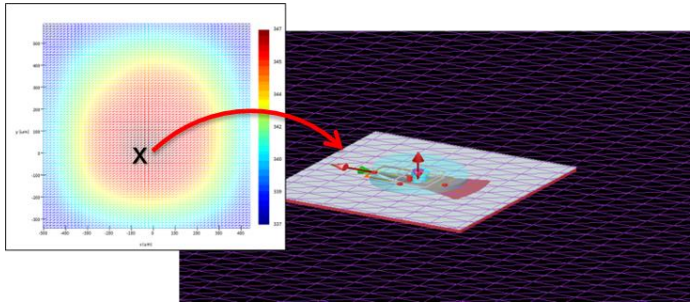
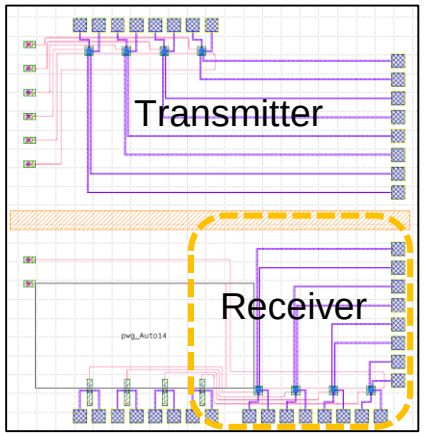
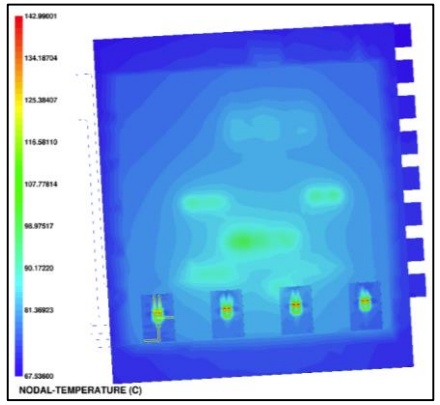


Figure: Importing temperature map into FDTD simulation of a grating coupler

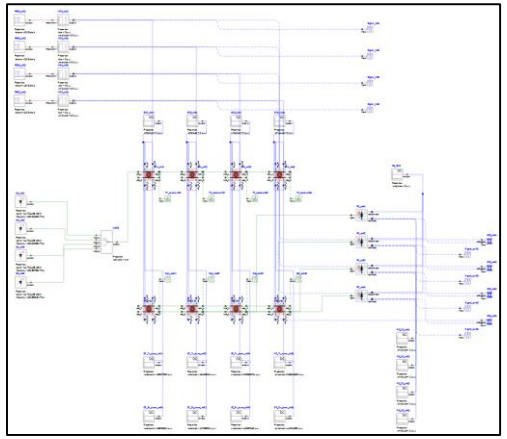
Layout of 4-channel WDM example circuit in PIC

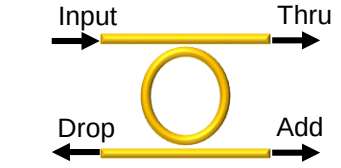


PIC temperature map of WDM receiver with thermal crosstalk from EIC

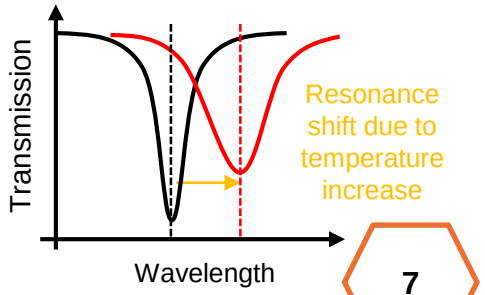


Schematic of 4-channel WDM circuit





Ring Resonator



Results: Thermal Simulation

- Performing steady-state thermal simulation with 15 mW thermal power applied to the heaters of the ring resonators in the EDM receiver.
- The value was set to half of the thermal power needed for a full FSR shift in the ring resonance with the assumption that it represents the average thermal power used by each right during operation.
- Temperature map from thermal simulation shows thermal crosstalk from PIC on EIC temperature profile and thermal crosstalk from EIC on PIC temperature profile. The PIC temperature map also captures thermal cross-talk between neighbouring rings.
- For thermal crosstalk, impact of EIC on PIC is more significant (subject to individual designs)

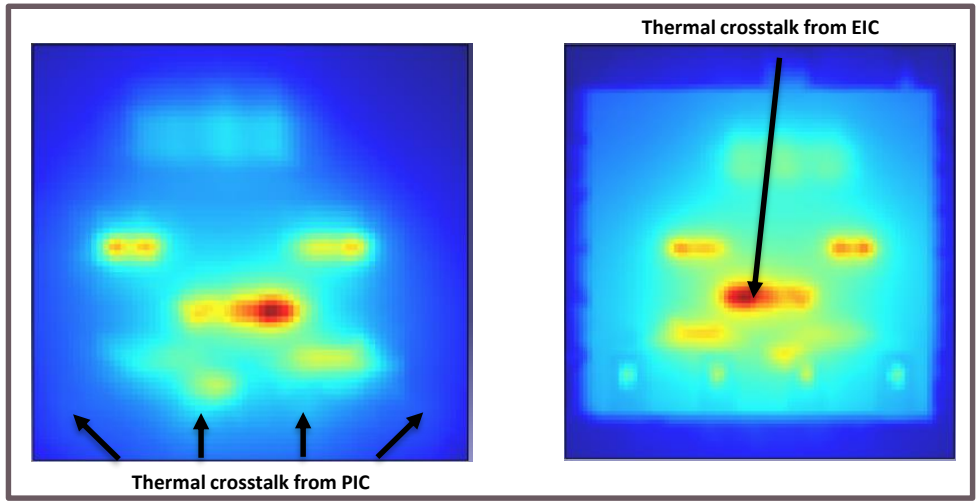


Figure: EIC bottom layer (left) and PIC top layer (right) temperature map

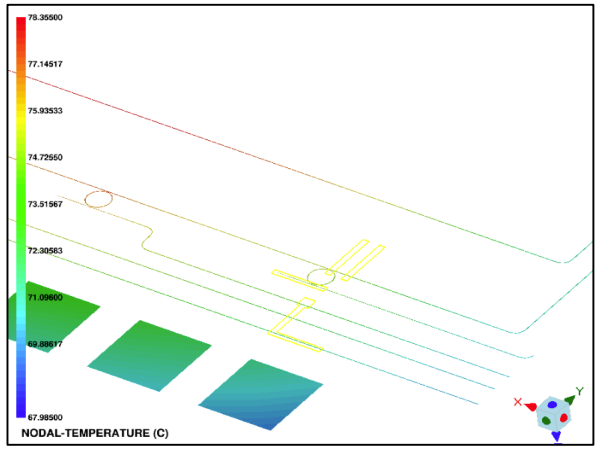


Figure: Accurate modeling of waveguide geometry in thermal simulation

Results: Thermally Aware PIC Design

- With temperature map imported, the resonant wavelength of the rings shift due to elevated temperature from thermal crosstalk and the eye diagram closes. (To find the cross-talk on each ring, individual simulations were performed with the corresponding ring heater turned off while keeping all other heat sources on.)
- Additional power needed on the thermal tuner to align the rings back to the channel wavelength and reopen the eye (e.g., 18.4 mW thermal power was applied to the ring resonator of channel 1).
- On a component level, investigation on a grating coupler simulation while importing temperature map from the thermal simulation reveals shift in insertion loss spectrum which can result in additional loss in circuit.
- Therefore, accurate thermal simulation of 3DIC package combined with thermally aware circuit simulation is needed when doing PIC design to properly estimate thermal budget.

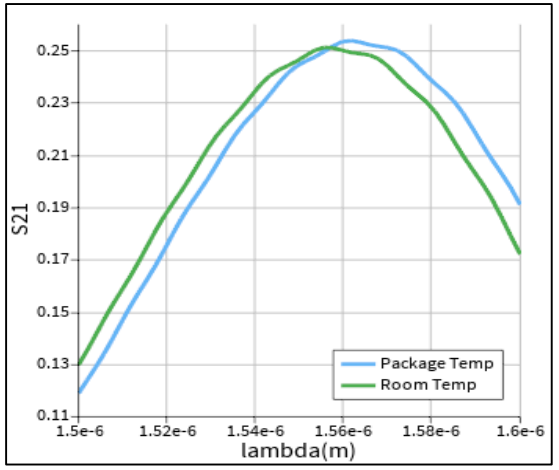


Figure: Shift in grating coupler spectrum due to elevated temperature from the package

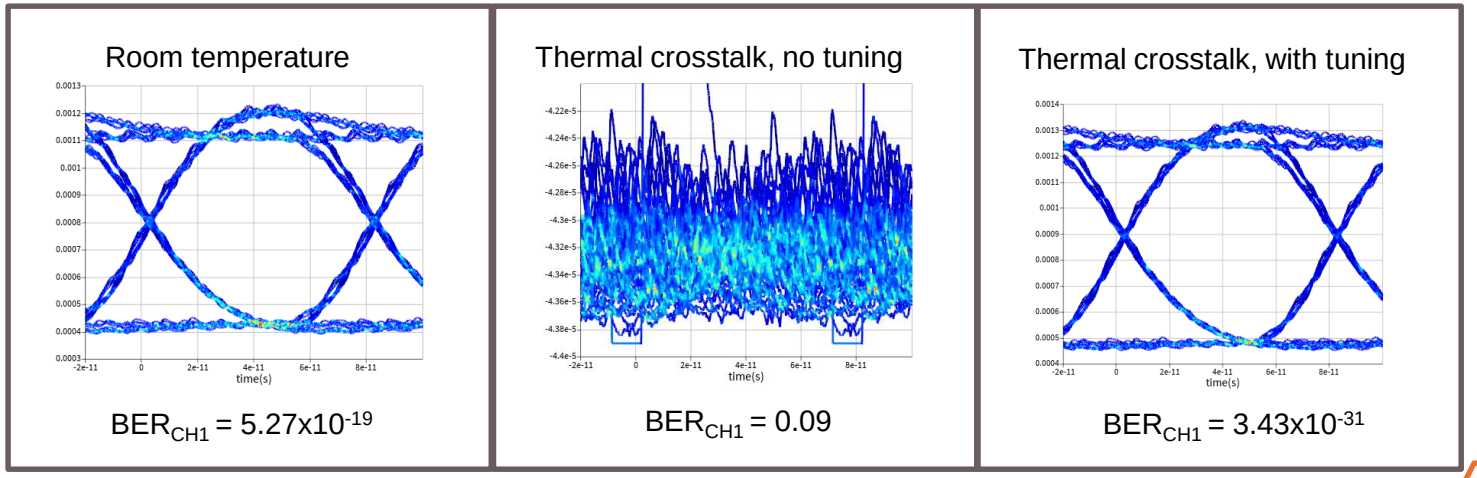


Figure: Eye diagram for channel 4 with BER values from different simulations.

Conclusion

- Demonstrated efficient and accurate thermal simulation of multi-die 3DIC package using chip thermal model (CTM).
- Hybrid approach for simulation of PIC die by complementing traditional CTM with photonic component geometry from GDS, e.g., heaters and waveguides.
- Simulation of full package enables modeling of thermal crosstalk between EIC - PIC and within PIC.
- Importing temperature map into photonic simulations enable thermally aware PIC design at both circuit and component level.